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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,211	02/03/2006	**Yimin Chen**	US030263	9664

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EXAMINER	
LE, TUNG X	
ART UNIT	**PAPER NUMBER**
2821	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,211	CHEN ET AL.	
	Examiner	Art Unit	
	TUNG X. LE	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/03/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' communication filed on February 03, 2006. In virtue of this communication, claims 1-18 are currently presented in the instant application.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 02/03/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The drawings submitted on 02/03/2006 are accepted.

Claim Objections

4. Claim 9 is objected to because of the following informalities:

Claim 9, line 1, "further" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Xia et al. (U.S. Patent No. 5,872,429).

With respect to claim 1, Xia discloses in figures 1-2 a ballast, comprising an inverter output stage [D]; and a power factor correction input stage [A-C] in electrical communication with the inverter output stage to apply a regulated DC voltage (having a pair of DC rails [RL1, RL2] to apply a DC output voltage to the inverter [E]) as a function (AC/DC) of a line voltage [RL1, RL2] to the inverter output stage, the power factor correction input stage including a power factor correction integrated circuit (figure 2a shows the power factor correction input stage including a power factor correction IC [U1]), and a line voltage sensing circuit [B, Q1, and R14-R15] in electrical communication with the power factor correction integrated circuit [U1] to apply a clamped rectified voltage (a DC outputted rectified voltage) to the power factor correction integrated circuit, wherein the clamped rectified voltage is a function (having a function related between the AC voltage source and the AC output voltage of the inverter applied to the lamp) of a load [LAMP] being applied by the inverter output stage to the power factor correction integrated circuit (figure 1).

With respect to claim 2, Xia discloses that wherein the clamped rectified voltage and the load being applied by the inverter output stage to the power factor correction integrated circuit are proportional (figure 2a shows a boost converter of the power factor correction circuit that the DC output voltage of the rectifier is being less than the DC output of the boost converter/PFC [C]; and the clamped rectified voltage is much smaller than the voltage applied to the lamp).

With respect to claim 3, Xia discloses in figure 1 that the ballast further comprises a dimming interface (having a dimming interface [I]) in electrical communication with the power factor correction input stage to communicate a dimming level signal (having a dimming signal [DIM] sent from the dimming interface to the controller [G]) as a function (a dimming controlling function for the lamp) of an external ballast control signal (having a dimming control signal from an external dimming controller, see column 6, lines 22-29), wherein the dimming level signal [DIM] is indicative of the load being applied by the inverter output stage to the power factor correction integrated circuit (figures 1 and 2b).

With respect to claim 4, Xia discloses that wherein the inverter output stage is in electrical communication with the power factor correction input stage to communicate a load feedback signal (having a load feedback signal via line [Z4]) to the power factor correction input stage; and wherein the load feedback signal is indicative of the load being applied by the inverter output stage [D] to the power factor correction integrated circuit (see figures 2a-2b).

With respect to claim 5, Xia discloses in figure 2a that the line voltage sensing circuit [B, Q1, and R14-R15] includes a voltage rectifier [B] operable to generate a rectified voltage (having a DC output voltage of the rectifier [B]) as a function of the line voltage (applying the DC output voltage to the PFC from an AC voltage source); a THD controller [Q1] operable to generate a clamping voltage (a DC output voltage applied to the inverter output stage) as a function (a correcting function) of the load being applied by the inverter output stage to the power factor correction integrated circuit; and a voltage divider [R14-R15] in electrical communication with the voltage rectifier and the

THD controller to generate the clamped rectified voltage as a function (a detecting function of the voltage applied to the lamp) of the rectified voltage and the clamping voltage (figures 2a-2b).

With respect to claim 6, Xia discloses in figure 2a that wherein the voltage divider includes a dividing node (having a dividing node disposed between the two resistors [R14 and R15]); and wherein the THD controller [Q1] includes means for applying the clamping voltage to the dividing node of the voltage divider as a function (having the dividing node electrically coupled to the controller [Q1] for applying the clamping voltage to the dividing node in order to correct a DC output voltage level applied to the inverter circuit) of the line voltage.

With respect to claim 7, Xia discloses that wherein the clamping voltage and the line voltage are inversely proportional (a DC voltage signal is being inversed from a AC voltage signal).

With respect to claim 8, Xia discloses that the ballast further comprises a dimming interface (having a dimming interface [I]) in electrical communication with the power factor correction input stage [A-C] to communicate a dimming level signal (having dimming level signals communicated between the pre-conditioner and the dimming interface) to the power factor correction input stage, the dimming level signal being indicative of the load being applied by the inverter output stage [D] to the power factor correction integrated circuit; and wherein the THD controller [Q1] includes means for generating the claming voltage as a function (a boosting correcting function to output a DC voltage applied to the inverter output stage [D]) line voltage (figure 1).

With respect to claim 9, Xia discloses that the ballast comprising wherein the inverter output stage [D] is in electrical communication with the power factor correction input stage [A-C] to communicate a load feedback signal (having a load feedback signal via line [Z4]) to the power factor to the power factor correction input stage; wherein the load feedback signal being indicative of the load [LAMP] being applied by the inverter output stage to the power factor correction integrated circuit; and wherein the THD controller [Q1] includes means for generating the clamping voltage as a function (a boosting correcting function to output a DC voltage applied to the inverter output stage [D]) of the load feedback signal (figures 1 and 2a-2b).

With respect to claim 10, Xia discloses that wherein the power factor correction integrated circuit including a multiplier input pin (the PFC integrated circuit [U1] shows a multi-input pin); and wherein the voltage divider [R14-R15] includes a dividing node (having a dividing node disposed between the two resistors [R14 and R15]) in electrical communication with the multiplier pin to apply the clamped rectified voltage to the power factor correction integrated circuit (see figure 2a).

With respect to claim 11, Xia discloses in figures 1-2a a power factor correction input stage [A-C], comprising a power factor correction integrated circuit [U1]; a line voltage sensing circuit [B, Q1, R14, and R15] in electrical communication with the power factor correction integrated circuit to apply a clamped rectified voltage (a DC output voltage from the rectifier [B]) as a function (a rectifying function) of a line voltage [RL1, RL2] to the power factor correction integrated circuit, wherein the clamped rectified voltage is a function (applying an input DC voltage to the inverter output stage to apply

an AC voltage to the load/lamp) of a load [LAMP] being applied to the power factor correction integrated circuit (figure 2a).

With respect to claim 12, Xia discloses that wherein the clamped rectified voltage and the load being applied to the power factor correction integrated circuit are proportional (figure 2a shows a boost converter of the power factor correction circuit that the DC output voltage of the rectifier is being less than the DC output of the boost converter/PFC [C]; and the clamped rectified voltage is much smaller than the voltage applied to the lamp).

With respect to claim 13, Xia discloses in figure 2a that the line voltage sensing circuit [B, Q1, and R14-R15] includes a voltage rectifier [B] operable to generate a rectified voltage (having a DC output voltage of the rectifier [B]) as a function of the line voltage (applying the DC output voltage to the PFC from an AC voltage source); a THD controller [Q1] operable to generate a clamping voltage (a DC output voltage applied to the inverter output stage) as a function (a correcting function) of the load being applied to the power factor correction integrated circuit; and a voltage divider [R14-R15] in electrical communication with the voltage rectifier and the THD controller to generate the clamped rectified voltage as a function (a detecting function of the voltage applied to the lamp) of the rectified voltage and the clamping voltage (figures 2a-2b).

With respect to claim 14, Xia discloses in figure 2a that wherein the voltage divider includes a dividing node (having a dividing node disposed between the two resistors [R14 and R15]); and wherein the THD controller [Q1] includes means for applying the clamping voltage to the dividing node of the voltage divider as a function

(having the dividing node electrically coupled to the controller [Q1] for applying the clamping voltage to the dividing node in order to correct a DC output voltage level applied to the inverter circuit) of the line voltage.

With respect to claim 15, Xia discloses that wherein the clamping voltage and the line voltage are inversely proportional (a DC voltage signal is being inversed from a AC voltage signal).

With respect to claim 16, Xia discloses that wherein the power factor correction integrated circuit including a multiplier input pin (the PFC integrated circuit [U1] shows a multi-input pin); and wherein the voltage divider [R14-R15] includes a dividing node (having a dividing node disposed between the two resistors [R14 and R15]) in electrical communication with the multiplier pin to apply the clamped rectified voltage to the power factor correction integrated circuit (see figure 2a).

With respect to claim 17, Xia discloses in figures 1-2 a ballast, comprising an inverter output stage [D]; and a power factor correction input stage [A-C] in electrical communication with the inverter output stage to apply a regulated DC voltage (having a pair of DC rails [RL1, RL2] to apply a DC output voltage to the inverter [E]) as a function (AC/DC) of a line voltage [RL1, RL2] to the inverter output stage, the power factor correction input stage including a power factor correction integrated circuit (figure 2a shows the power factor correction input stage including a power factor correction IC [U1]), and means for applying a clamped rectified voltage (having a line voltage sensing circuit [B, Q1, R14-R15] being means for applying a function) to the power factor correction integrated circuit, wherein the clamped rectified voltage is a function (having

a function related between the AC voltage source and the AC output voltage of the inverter applied to the lamp) of a load [LAMP] being applied by the inverter output stage to the power factor correction integrated circuit (figure 1).

With respect to claim 18, Xia discloses in figures 1-2a a power factor correction input stage [A-C], comprising a power factor correction integrated circuit [U1]; means for applying a clamped rectified voltage (having a line voltage sensing circuit [B, Q1, R14-R15] being means for applying a function) as a function (a rectifying function) of a line voltage [RL1, RL2] to the power factor correction integrated circuit, wherein the clamped rectified voltage is a function (applying an input DC voltage to the inverter output stage to apply an AC voltage to the load/lamp) of a load [LAMP] being applied to the power factor correction integrated circuit (figure 2a).

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Nemirow et al. (U.S. Publication No. 2005/0012467 A1) discloses a fluorescent lamp electronic ballast.

Prior art Ribarich (U.S. Publication No. 2004/0012347 A1) discloses a single chip ballast control with power factor correction.

Prior art Newman, JR. et al. (U.S. Publication No. 2003/0107332 A1) discloses a single switch electronic dimming ballast.

Inquiry

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUNG X. LE whose telephone number is (571)272-6010. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Owens can be reached on 571-272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Douglas W Owens/
Supervisory Patent Examiner, Art Unit 2821
July 20, 2008